### **WEST Search History**

Hide Items Restore Clear Cancel

DATE: Tuesday, April 19, 2005

Hide?	<u>Set</u> <u>Name</u>	Query	<u>Hit</u> Count			
DB=PGPB,USPT; PLUR=YES; OP=ADJ						
	L16	L15 or l14	18			
	L15	L13 and 110	4			
	L14	L13 and 111	14			
	L13	20000417	307			
	L12	(first (device or computer)) near8 (second (device or computer)) near8 (interface or( front end))	663			
	L11	(format or reformat or convert or converting or transform) near6 (request or response or traffic) near20 (intermediate or proxy or device)	3329			
	L10	(translate or translating) near5 language	3830			
DB=PGPB, USPT, USOC, EPAB, JPAB, DWPI, TDBD; PLUR=YES; OP=ADJ						
	L9	20000417	3047			
	L8	(translate or translating) near5 language	5673			
	L7	20000417	2123			
	L6	(format or reformat or convert or converting or transform) near6 (request or response or traffic) near20 (intermediate or proxy or device)	4332			
$\blacksquare$	L5	(format or reformat or convert or converting or transform) near6 (request or response or traffic)	38484			
	L4	(format or reformat or convert or converting or transform) near6 (request or response)	35808			
	L3	20000417	50571			
	L2	20000417	0			
	Ll	(convert or converting or transform or transforming or converter or conversion) near8 (protocol or format or language or translate or translation)	94878			

END OF SEARCH HISTORY

## **WEST Search History**

Hide Items Restore Clear Cancel

DATE: Tuesday, April 19, 2005

Hide?	Set Name	Query	Hit Count		
	DB=PGPB, US	$PT,USOC,EPAB,JPAB,DWPI,TDBD;\ PLUR=$	YES; OP=ADJ		
	L8	20000417	35		
	L7	(content conversion).ti.	95		
	DB=PGPB,USPT; PLUR=YES; OP=ADJ				
	L6	20000417	14		
	L5	(content conversion).ab.	27		
	L4	20000417	. 0		
	L3	(content conversion).ti.	6		
	L2	20000417	411		
	L1	content conversion	800		

**END OF SEARCH HISTORY** 

Previous Doc Next Doc Go to Doc# First Hit

Generate Collection

L8: Entry 1 of 35

File: JPAB

Aug 24, 2001

PUB-NO: JP02001229106A

DOCUMENT-IDENTIFIER: JP 2001229106 A TITLE: CONTENTS CONVERSION SYSTEM

PUBN-DATE: August 24, 2001

INVENTOR-INFORMATION:

NAME

COUNTRY

KONDO, TAKESHI

TAKAHASHI, YASUHIRO

INT-CL (IPC):  $\underline{G06} + \underline{13}/\underline{00}$ ;  $\underline{G06} + \underline{12}/\underline{00}$ 

#### ABSTRACT:

PROBLEM TO BE SOLVED: To solve the problem that requested contents which exceed the limit of reception capacity can not be serviced to a portable terminal side by Web service to a portable terminal has a limit of single-time reception capacity.

SOLUTION: An original content acquisition agent means, a content division condition acquiring means, a content dividing means, a means which generates a link between subcontents as the divided contents, a storage means for the subcontents, and a sending-back means for the subcontents are provided between the portable terminal and a Web server.

COPYRIGHT: (C) 2001, JPO

Previous Doc Next Doc Go to Doc#

# Previous Doc Next Doc Go to Doc# First Hit Fwd Refs

Generate Collection

L16: Entry 17 of 18 File: USPT Jul 26, 1994

DOCUMENT-IDENTIFIER: US 5333198 A TITLE: Digital interface circuit

#### Abstract Text (1):

A digital interface for allowing a first device which receives and sends information serially to communicate with a second device which receives and sends information in parallel. The first device may be an encryption unit while the second device may be a relay/responder/reporter connected to a transmitter or a digital signal processing unit. The digital interface comprises an erasable programmable logic device which during an uplink data transfer performs the function of converting parallel logic signals, that is control signals and data words provided by the relay/responder/reporter, for example, to commands and data to be transmitted by a transmitter serially to the encryption unit. In a like manner, the erasable programmable memory device during a downlink data transfer converts serial commands and data received from the encryption unit by a receiver to a parallel format for transmission to the relay/responder/reporter. The protocol converter includes a dual port memory which is used for temporary storage of data during an information transfer from the encryption unit to the relay/responder/reporter. The protocol converter also includes a programmable array logic device for latching therein commands which are sent to the encryption unit and commands received from the encryption unit during a data transfer and a microcontroller which monitors the commands latched in the programmable array logic device. When the microcontroller fails to detect a send or receive command during an uplink or down link data transfer, the microcontroller will reset the protocol converter allowing for a restart of the data transfer.

## <u>Application Filing Date</u> (1): 19930527

#### Brief Summary Text (12):

The subject invention overcomes the disadvantages of the prior art including those mentioned above in that it comprises a digital <u>interface circuit/protocol converter for allowing a first device which receives and sends information serially to communicate with a second device which receives and sends information in parallel. The first device may be an encryption unit or a second protocol converter, while the second device may be a relay/responder/reporter connected to a transmitter, a digital signal processing unit or a radio frequency (RF) input/output (I/O) logic unit.</u>

#### Detailed Description Text (29):

Referring now to FIGS. 2, 7A-7W, 8a-8c, 14, 15 and 16 when encryption unit 53 provides a request to send command (hexadecimal 3) to protocol converter 55, receiver 81, FIG. 3d, will convert the request to send command from serial to parallel and then supply the request to send command to the RTCO-RTC3 inputs of erasable programmable logic device 89. The request to send command is first provided to receive command decode circuit 119 which decodes the command resulting in its R.sub.-- RTS output transitioning to the logic one state. The logic one is supplied through the R.sub.-- RTS input of command receive circuit 117, OR gate 319, AND gate 321 to the clock input of D Flip-Flop 323 clocking the logic one at

the D input of Flip-Flop 323 to its Q output. It should be noted that AND gate 321 is enabled since the Q output of D Flip-Flop 325 is at the logic zero state which then is inverted by inverter 327 resulting in the logic one being supplied to AND gate 321.

#### Detailed Description Text (171):

From the foregoing, it may readily be seen that the subject invention comprises a new, unique and exceedingly useful interface which may be used to allow for communication between a first device which sends and receives data in a serial format and a second device which sends and receives data in a parallel format. Obviously, many modifications and variations of the present invention are possible in light of the above teachings. It is therefore to be understood that within the scope of the present claims the invention may be practiced otherwise than as specifically described.

Previous Doc Next Doc Go to Doc#